51357/SDB/B600

WHAT IS CLAIMED IS:

    1.   A first-in-first-out (FIFO) circuit comprising:

5   a plurality of FIFO registers;

    a write pointer circuit having an input that receives a write clock signal and a plurality of outputs that respectively couple to the plurality of registers, the write pointer circuit generates a write pointer signal at a first

10   frequency; and

    a read pointer circuit having an input that receives a read clock signal and a plurality of outputs that respectively couple to the plurality of registers, the read pointer circuit generates a read pointer signal at a second frequency that is

15   different than the first frequency.

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